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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,867	01/29/2002	Toru Okabayashi	1081.1136	8441

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EXAMINER	
MATTHEW, AARON D	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,867	OKABAYASHI ET AL.	
	Examiner	Art Unit	
	Aaron D Matthew	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-12, and 16* is/are allowed.

6)☒ Claim(s) *1, 2, and 13-15* is/are rejected.

7)☒ Claim(s) *3-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

1. The drawings are objected to because the word, "instruction", is misspelled, "instruction", in Fig. 7, elements P20, P22, and P26; and in Fig. 9, element P44. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR

1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. The disclosure is objected to because of the following informalities:
   - Line 11 of page 1 should be changed to read, "(ICE) which stores a program ~~s~~ and data for debugging and whose";
   - It is unclear as to what is meant by the language on lines 9-10 of page 3, "tool bus cannot have a large number of multiple-bit structure like the data bus";
   - The examiner suggests that lines 7-8 of page 15 should be changed to read, either, "even if subsequent instruction fetch request signals have not been received," or, "even if a subsequent instruction fetch request signal has not been received";

- The language on lines 5-6 of page 15, "an instruction address containing a branch less is incremented in steps of two", is confusing; examiner suggests replacing "branch less" with "branchless signal".

Appropriate correction is required.

4. Claims 1-16 have been examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Somasundaram et al, (US. 5,491,793), and further in view of Higashida, (U.S. 6,233,673 B1).

Regarding claim 1, Somasundaram teaches a microcontroller comprising;

- A CPU, (see col. 2, line 35);
- A bus controller, (see col. 3, lines 60-64);

- An instruction address bus and an instruction code bus, (see col. 4, lines 61-65), of a first bit number, (see col. 3, lines 37-40), which connect said CPU and bus controller; and
- A debug support unit, which is connected to said instruction address bus and instruction code bus, (see Fig. 1, element 130);
- Wherein said debug support unit is connected to a diagnostic instrument via a tool bus, (see Fig. 1, element 140), whose bit number is smaller than said first bit number, (See col. 5, lines 45-50), and via a bus status signal line which reports on the status of the tool bus, (see Fig. 5, and note col. 8, lines 63-65); and
- Wherein said debug support unit comprises:
    i. A parallel to serial conversion circuit, which performs parallel to serial conversion of an instruction address, (see col. 6, lines 1-10);
    ii. A status information generation circuit, which generates a status information signal, (again, see Fig. 5, and note col. 8, lines 63-65), which contains branch information, (see, "I-PLUS-4", in col. 8, lines 58-62, and note col. 7, lines 1-5), and an instruction fetch request, (see, "IFETCH", in col. 8, lines 58-62), in response to a branch signal and instruction fetch request signal received from said CPU, (Figs. 1 and 5, show that said signals are received from said CPU);
    iii. A status output circuit, which outputs an instruction address output signal to said bus status signal line in response to the status

information signal, (see col. 8, lines 53-57: the MSN signal is herein interpreted as an instruction address output signal as it contains information related to the output of an instruction address); and

iv. A data output circuit, (see Fig. 5), which, in response to said status information signal, when said branch information contains a branch, outputs said converted instruction address in series to said tool bus, (note col. 6, lines 1-10), and when the branch information contains no branch outputs a branchless signal to said tool bus, (note col. 7, lines 40-67, wherein the signal "I-PLUS-4" is a signal sent when no branch is performed, and also note that the instruction address is only required to be sent when said signal is not active).

Somasundaram fails to teach that said diagnostic instrument is an external in-circuit emulator. However, Somasundaram does teach that said diagnostic instrument is used both to trace the operations of the CPU and to provide instructions used in the debugging of the CPU, (see Abstract).

Higashida teaches an external in-circuit emulator used to support the debugging of a CPU, (see col. 1, lines 5-10), which comprises a bit-width converter for converting the CPU internal signal into a plurality of reduced bit-width signal for outputting to the ICE in multiple cycles, (see col. 2, lines 29-37).

Higashida and Somasundaram are analogous art because they are from the same field of endeavor, viz., external support for a CPU debugging operation facilitated by bit-width conversion means.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the teachings in order to achieve a microcontroller, as described in Somasundaram, which is supported in a debugging operation by the external in-circuit emulator of Higashida.

One of ordinary skill in the art would have been motivated to combine the teachings because the ICE of Higashida meets an explicitly stated need of the microcontroller debugging system of Somasundaram. Somasundaram states that the diagnostic instrument is needed in the system to trace CPU operations, and to provide instructions for debugging the CPU, (see, again, Abstract). The ICE of Higashida is a conventionally recognized means of both tracing CPU operations and providing instructions for debugging the CPU. Therefore, one of ordinary skill in the art would have been clearly motivated to substitute the external ICE of Higashida for the diagnostic instrument of Somasundaram, in order to provide a conventionally recognized means of fulfilling the requisite functionality of said instrument.

Claim 13 is rejected because it recites limitations similar to claim 1, note the discussion above regarding claim 1. Also note that Somasundaram teaches the following: In a case in which an instruction fetch request, (note col. 8, lines 58-62 in which "IFETCH" indicates whether an instruction fetch is being performed), received from said CPU is an instruction with a branch, (see col. 6, lines 33-36), said debug support unit performs parallel to serial conversion of the instruction address, and then outputs the converted instruction address to said tool bus in series, (see col. 6, lines 1-10), and, in a case in which said instruction fetch request is a branchless instruction, outputs a branchless signal to said tool bus, (see col. 7, lines 50-67).

Regarding claim 2, Somasundaram teaches a microcontroller, as described in reference to claim 1, wherein said data-output circuit outputs said converted instruction address in series to said tool bus in a plurality of cycles when said branch information contains a branch, (see col. 6, lines 33-36 and 1-10), and outputs said branchless signal to said tool bus in a single cycle when the branch information contains no branch, (see col. 6, lines 21-28 and col. 7, lines 40-67).

6. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Somasundaram, in view of Higashida, as applied to claim 1 above, and further in view of Dwyer, III, (U.S. 6,430,682 B1).

Claim 14 is rejected because it recites limitations similar to claim 1, note the discussion above regarding claim 1, in additional consideration of the following:

Somasundaram teaches that the debug support unit outputs said instruction address to said tool bus in series in response to an instruction fetch request signal received from said CPU, (see col. 12, lines 4-5, and col. 11, lines 8-15), and receives instruction code, which corresponds to the instruction fetch request, from said in-circuit emulator, (see col. 12, lines 6-9).

Somasundaram fails to teach that the debug support unit initiates instruction-prefetch control when instruction code, which corresponds to the instruction fetch request, has been received from said in-circuit emulator, before a next instruction fetch request is received.

Dwyer teaches a processor that initiates instruction-prefetch control when instruction code, which corresponds to a first instruction fetch request, has been received, before a next instruction fetch request is received, (see col. 1, lines 17-22, and 43-45).

Dwyer and Somasundaram are analogous art because they are from the same field of endeavor, viz., systems that enable the access of instruction code in computer processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the instruction prefetching of Dwyer with the instruction fetch request operations of the debug support unit in Somasundaram, in order to achieve an improved means of fetching instructions through said debug support unit, utilizing instruction prefetching.

One of ordinary skill in the art would have been motivated to combine the teachings because the instruction prefetching technique, disclosed in Dwyer, meets an explicitly recognized need in the field of processor instruction retrieval. Dwyer states, (note col. 1, lines 10-15), that one method of increasing the effective rate of processor execution is by prefetching. Therefore, one of ordinary skill in the art would have been clearly motivated to utilize instruction prefetching in the debug support unit of Somasundaram, in order to improve the rate at which said unit is capable of executing instruction fetch request operations.

Regarding claim 15, see Dwyer, col. 1, lines 35-38. Also note that Somasundaram teaches sending a branch instruction address to said tool bus in series, (note col. 6, lines 1-10).

Allowable Subject Matter

7. Claims 6-12 and 16 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 6-10, the limitation, "wherein, when said status information generation circuit finishes receiving instruction code which corresponds to a current instruction fetch request before receiving a next instruction fetch request, the status information generation circuit generates a prefetch status information signal for an instruction-prefetch request with an instruction address which succeeds the instruction address of the current instruction fetch request," in combination with the other limitations in the claim, was not found in any prior art.

Regarding claims 11-12, the limitations of, "an encoder, which outputs an encoded address which includes an effective address contained in an address and an effective digit number signal for the effective address; and, a status information

generation circuit, which, in a period of the number of cycles corresponding to said effective digit number, generates a status information signal which contains an instruction fetch request or data access request, in response to an instruction fetch request signal or data access request signal, respectively received from said CPU," in combination with the other limitations in the claim, were not found in any prior art.

Regarding claim 16, the limitation, "wherein said debug support unit comprises a data output circuit, which generates an encoded address which includes an effective address contained in an address and an effective digit number signal for the effective address, and which outputs said encoded address to said tool bus in series in response to an instruction fetch request signal or data access request signal received from said CPU," in combination with the other limitations in the claim, was not found in any prior art.

9. Claims 3-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Allison et al, (U.S. 5,053,949), teaches a microcontroller comprising a debug support unit that communicates with an external in-circuit emulator to facilitate debugging operations.
- Utsumi, (U.S. 6,493,833 B1), teaches a microcontroller with a built-in debugging circuit capable of executing an evaluation program utilizing an external in-circuit emulator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron D Matthew whose telephone number is (571) 272-3662. The examiner can normally be reached on Mon-Fri, from 8:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aaron D Matthew
Examiner
Art Unit 2114

ADM

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